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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,137	10/21/2003	David H. Asher	200301840-2	3633

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 08/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,137	ASHER ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13-15 and 19-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on October 21, 2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5, 7-9, 13-15, 19-20 and 22-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burger et al (US Patent No. 6,965,969) and Chudnovsky et al (US Patent No. 6,381,669).

For claim 1, Burger discloses a novel architecture for set associative cache, comprising:

a set associative cache having a plurality of ways wherein the ways are segmented into a plurality of banks and wherein a first way has a fast access time (a plurality of independently accessible memory banks may be organized into an n-way set-associative cache memory including m-spread bank sets; each way of the n-ways may have a different access latency, col. 11, lines 7-17; latencies to access all bank

sets are not the same, some bank sets will be faster than others, col. 6, lines 10-13; banks closer to the cache controller and/or processor may incur lower latency, col. 2, lines 64-65);

access control logic which manages access to the cache and is coupled to said plurality of ways (cache control circuitry coupled to the arithmetic functional unit, and a plurality of independently accessible memory banks coupled to the cache control circuitry, col. 11, lines 21-28); and

a plurality of muxes coupled to said first way in each of said banks and coupled to said access control logic (data can be accessed at each sub-bank and returned to output drivers after passing through multiplexers, where the requested line is assembled and driven to the cache controller, col. 1, lines 35-39).

Burger fails to disclose the remaining claim limitations.

Chudnovsky, however, helps disclose the access control logic controls the mux in a bank to remap any defective way in a bank to the first way in that same bank (a remapping and scrambling system enables fault tolerant operation of a memory system and fault tolerant operation of multi-processor and multi-bank systems, col. 17, lines 47-50; once testing is performed and defective elements such as memory blocks, banks, or processing units are found, defect information is stored and used by remapping circuitry, col. 17, lines 64-67).

Burger and Chudnovsky are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include

remapping defective ways in a bank to the first way of the bank using multiplexers because this would enable fault tolerant operation of the whole memory system and fault tolerant operation of multi-processor and multi-bank systems on-a-chip (col. 17, lines 48-50), as taught by Chudnovsky.

Claim 2 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 3, the combined teachings of Burger and Chudnovsky disclose the invention as per rejection of claim 1 above.

Chudnovsky further helps disclose self test logic coupled to said access control logic to test the cache for defects (this testing can be internal, using various state of the art approaches, such as a built-in-self-test, col. 17, lines 57-63).

For claim 4, the combined teachings of Burger and Chudnovsky disclose the invention as per rejection of claim 3 above.

Chudnovsky further helps disclose said self test logic tests the cache for defects on power up (both the testing and reprogramming can be done following boot procedures, col. 18, lines 11-15).

For claim 5, the combined teachings of Burger and Chudnovsky disclose the invention as per rejection of claim 3 above.

Chudnovsky further helps disclose said self test logic stores the location of defects in a status register (following boot procedures the software tests the memory and downloads the list of bad elements into a RAM or register, col. 18, lines 13-15).

For claim 7, the combined teachings of Burger and Chudnovsky disclose the invention as per rejection of claim 1 above.

Burger further helps disclose said set associative cache has a data array having a plurality of ways wherein the ways are segmented into a plurality of banks and wherein a first way has a faster access time (a distributed cache array, in which tags are distributed with the banks, col. 7, lines 17-18; each bank may also include a plurality of sub-banks, one or more tag arrays, col. 3, lines 55-56).

Claim 8 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 9 is rejected using the same rationale as for the rejection of claim 1 above.

For claim 13, the combined teachings of Burger and Chudnovsky disclose the invention as per rejection of claim 1 above.

Burger further helps disclose a microprocessor die (apparatus, systems, and methods for implementing a cache memory in a computer system and utilizing cache memories having a plurality of accessible banks, col. 1, lines 16-20).

Claim 14 is rejected using the same rationale as for the rejections of claims 2 and 13 above.

Claim 15 is rejected using the same rationale as for the rejections of claims 9 and 14 above.

Claim 19 is rejected using the same rationale as for the rejection of claim 1 above.

Claim 20 is rejected using the same rationale as for the rejections of claims 3 and 19 above.

Claim 22 is rejected using the same rationale as for the rejection of claim 19 above.

Claim 23 is rejected using the same rationale as for the rejections of claims 15 and 22 above.

Claim 24 is rejected using the same rationale as for the rejection of claim 13 above.

4. Claims 6 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burger et al (US Patent No. 6,965,969), Chudnovsky et al (US Patent No. 6,381,669) and Rowlands et al (US Patent No. 6,748,492).

For claim 6, the combined teachings of Burger and Chudnovsky disclose the invention as per rejection of claim 5 above.

These teachings fail to disclose the limitations of the current claim.

Rowlands, however, helps disclose said access control logic reads the location of defects in the cache from the status register to determine proper control of said muxes (a combination of direct access transactions and deterministic setting may be used to provide cache testing by using a direct access transaction to select a test way, then using a memory transaction which misses the cache to cause test data to be loaded into the test way; a subsequent direct access transaction may then read the data from the test way to check the test data for correct storage in the selected entry, and the tag information may be captured in a register within the cache, which may be read from the register and checked for accuracy, col. 2, lines 50-59; the tag register outputs the data stored therein to a mux; decoder provides the selection control to a mux, and selects the data from data memory; the decoder decodes the address of a transaction and, if

the address is the address to which the tag register is mapped, the decoder selects the contents of the tag register via a mux, col. 11, lines 23-31).

Burger, Chudnovsky and Rowlands are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include reading the location of defects in a cache from the status register because defect information would allow for effiecient use by the remapping circuitry (col. 17, lines 66-67), as taught by Chudnovsky.

For claim 21, the combined teachings of Burger and Chudnovsky disclose the invention as per rejection of claim 19 above.

These teachings fail to disclose the limitations of the current claim.

Rowlands, however, helps disclose a step of disabling a way in a bank when that way is defective (a way is established as a way to be selected for eviction responsive to performing a transaction, col. 3, lines 20-22).

Citation of Pertinent Prior Art

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Olarig et al (US Patent No. 5,835,948) discloses a multiple-way cache implemented in a single bank memory, where an address line of a single bank of memory is used to select between ways.

Lyon (US PGPub No. 20030154345) discloses a unified tag subsystem for a multilevel cache memory system, including a tag index for indexing a tag memory which has way-specific address tags.

Puri et al (US PGPub No. 20030196143) discloses a controller circuit including built-in self-test and built-in self-repair modes of operation, and memory blocks may be remapped.

Contact Information

6. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

7-27-06

Mano Padmanabhan 8/6/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER